Reg. No. :

Question Paper Code : 11300

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2011

Sixth Semester

Electronics and Communication Engineering

EC 2354 — VLSI DESIGN

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions

PART A — (10 × 2 = 20 marks)

1. Draw the energy band diagrams of the components that make up the MOS system.

2. What is body effect coefficient?

3. What is the influence of voltage scaling on power and delay?

4. Express T_{PHL} and T_{PLH} in terms of C_{load} .

5. Draw the circuit diagram of a CMOS bistable element and its time domain behavior.

6. Write a note on CMOS transmission gate logic.

7. Write a note on partition and MUX technique.

8. List the design guidelines for I_{DDQ} testing.

9. What is transport delay model?

10. What is subprogram overloading?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain in detail with a neat diagram the fabrication process of the nMOS transistor. (8)

(ii) Discuss in detail with a neat layout, the design rules for a CMOS inverter. (8)

Or

(b) (i) Discuss in detail with necessary equations the operation of MOSFET and its current- voltage characteristics. (11)

(ii) Explain briefly CMOS process enhancements. (5)

12. (a) Explain in detail about

(i) Channel length modulation. (6)

(ii) Constant field scaling. (5)

(iii) Constant voltage scaling. (5)

Or

(b) With necessary equations, explain in detail about :

(i) Short current effect. (8)

(ii) Narrow channel effect. (8)

13. (a) (i) For a resistive load inverter circuit with $V_{DD} = 5V, K_n' = 20\ \mu A/V^2$, $V_{TO} = 0.8V, R_L = 200\ k\Omega$, and $\frac{W}{L} = 2$. Calculate the critical voltages on the voltage transfer characteristics and find the noise margins of the circuit. (6

(ii) Explain the detail about pseudo- nMOS gates with neat circuit diagram. (10)

Or

(b) (i) Design a transistor level schematic of the one bit full adder circuit and explain. (6)

(ii) Discuss in detail the characteristics of CMOS transmission gate.(10)

14. (a) Explain in detail the sequence of Scan- Based techniques. (16)

Or

(b) With the essential circuit modules, explain in detail the BIST technique. (16)

15. (a) (i) How is component instantiations bound? Explain it using a one bit full adder circuit? (6)

(ii) What is incremental binding? Explain with an example. (5)

(iii) Explain Gate level modelling with a suitable example. (5)

Or

(b) (i) What are the main purposes of text bench? (8)

(ii) Write a note on waveform generation? (5)

(iii) Write VHDL coding for a decoder circuit :

(1) Dataflow model.

(2) Behavioral model. (3)

———————