B. E. Part II (CST) 4th Semester Examination, 2006

Subject: Computer Organization — Paper: CST-402
Time: 3 hours — Full marks: 100

Answer any 4

1. a) Explain frequency dependent opcode optimization scheme. 10

b) A m/c is being designed whose instructions range from 1 to 6 bytes in width, with 2-bytes instruction being most common and 5- or 6-byte instruction rarely used. Compare the following opcode encoding schemes-

i. The leftmost 3 bits in the first byte of every instruction contains a binary number (1 to 6) that indicates the width of the instruction in bytes.

ii. One-byte instructions begin with 0 in the leftmost bit position of the first byte, 2-byte instructions begins with 10, and all other instructions begin with 11 followed by a 2-bit field that indicates the number of additional bytes (beyond the third) in the instruction. 10

c) Explain how Program Counter (PC) can be utilized in optimizing the instruction length. 5

2. a) Show the adder-sub tractor circuit that must be incorporated with a full adder. 5

b) State Booth's algorithm for multiplication of two 2's complement numbers. Explain the execution steps of Booth's algorithm with an example. Describe the limitations of Booth's algorithm. 20

3. a) Show how 2k X 8 SRAM chips can be used to build a 4k X 16 memory unit. 10

b) What do you mean by memory folding ? A CPU is having 16 address lines, data bus, RD, WR, and other normal signal lines. Interface one 8k byte and one 4k byte RAM chips with the CPU avoiding memory folding. Identify the memory address space occupied by the memory chips. 15

4. a) The first access to af'any cache block/page results *in* a miss, and called "compulsory misses' - "these are truely compulsory only if we follow on-demand fetching" - Explain. 6

b) A program accesses each element of a 1024X1024 matrix 8 times in each course of its execution. If the data cache can accommodate 256 matrix elements and 16 matrix elements per block/page, then how many compulsory data cache misses will be caused by this program's execution ? 7

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c) Note the various parts of the address (Figure *x), in a memory system, that identify the tag bits, set index in cache, and word offset to access the 2-way set-associative cache. 12

Estimate the volume of memory, cache block size in words and the volume of cache of this memory system.

5. Write microprogrames to emaluate the single-address instructions LOAD X, STORE X, AND X and JUMP X. Briefly describe the design steps of a hardwired control unit. Point out the limitations of such a design. 25

6. a) Describe the DMA data transfer scheme from an Input device to the Main memory. Identify the role of a CPU in DMA data transfer. 15

b) Describe the instruction pipeline architecture with four stages. Calculate the speed up factor of the pipeline system compared to that of equivalent nonpipelined processor. 10

7. Give the detailed design (any two) of the following: 25
   a) Carry Look Ahead adder
   b) Interleaved memory system
   c) Match logic of one word in an associative memory