B. E. Part-Hi (CST) Final EjiWraflon,

Subject: Computer Architecture — Paper: CST-502

Time: 3 hours — Full marks: 100

Answer any four

1. Define non-linear pipeline. The following reservation table

Si	*X*					*X*
S2		X		X		
S3			X			
				X	X	

is for a 4-stage (Si, S2, S_3, and S_4) non-linear pipeline.

a) Find out forbidden latencies of this pipeline and the MAL & lower bound of MAL. 15

b) Insert one non-compute delay stage into the pipeline to make a latency 1 permissible. Show the modified reservation table and the collision vector of modified pipeliner. 10

2. a) Consider a cache (Ml) and memory (M2) hierarchy, where

Ml: 16 K words, 50 ns access time

M2: 1M words, 400 ns access time

Assuming 16 word cache blocks and a set size of 128 words with set-associative mapping: (i) show the mapping between M2 & Ml and the address bits that identify the tag field, the set number and the word number,

(ii) calculate the effective memory access time with a cache hit ratio of 0.90.

Explain how cache set size affects the hit ratio. 15

b) Define CPI. In a 16-stage superpipeline 4 bubbles must be inserted for conditional branch instructions. The branch instructions constitute 15% of all instructions executed. About 2% of all instructions encounter a cache miss when accessing the data memory, causing the pipeline to stall for 25 cycles. Compute effective CPI for this pipeline. 10

3. What do you mean by "exceptions'? Explain a case of out-of-order exceptions and the methodology for handling it in instruction pipeline. **25**

4. a) Show how the following loop can be parallelized despite the obvious loop-carried dependency. State the assumptions taken.

```
for i=l to 15 do
    a[i]    := a[i] + b[i];
    b[i+l]  := c[i] + d[i]
endfor'
```

10

b) A program consists of two nested loops with a single branch instruction at the end of each loop and no other branch instruction anywhere. The outer loop executed 10 times and the inner loop executed 20 times. Determine the accuracy of the following prediction strategies

- i) predict taken, and ii) use 1-bit of history. 15

5. a) What do you mean by cache coherence problem in a multiprocessor system? A cache coherence protocol (updating) updates the other (P-l) copies of a cache line when one shared copy is modified. It prevents some future cache misses. Discuss which approach, updating or invalidation, is lead to better performance with each of the following access patterns to variable V.

i) Repeat a number of times: processor PI writes a new value into V and all other (P-!) processors read the new value, ii) Repeat a number of times: processor PI writes *m* times into V; this is followed by

processor P2 reading the value of V.

State the assumptions taken. 15

b) Draw a data flow graph showing the computations of

```
if a<b then a*b
   else a-b
endif.
```

10

6. Write short notes on-

a) Reduction computer, and 10

b) CRCW Shared Memory SEVID machine. 15