

B.E. (CST) Part-IV 8th Semester Examination, 2006

Digital System Design & Implementation
(CST-803/5)

Time : 3 hours

Full Marks : 100

Answer any FIVE questions.

1.

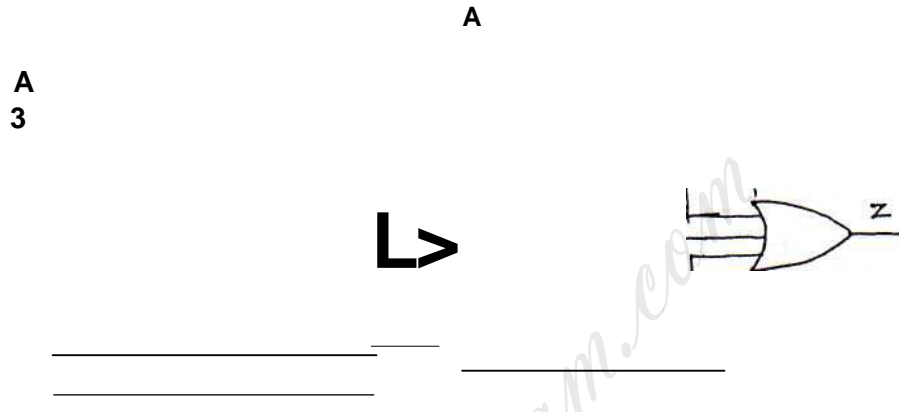


Fig.-1

- a) Find the set of all tests that detect the fault a s-a-0.
- b) Find the set of all tests that detect the fault b-s-a-(
- c) Find the set of all tests that detect the multiple fault {a s-a-0, b s-a-0}
- d) Find a circuit that has an undetectable stuck fault. [5+5+5+5]

2.

- a) Mention the major advantages of PLA design.
- b) Find minimal cost of PLA design using column folding and block folding technique of following functions,
 $F_1 = B + CE + ADE$
 $F_2 = AD + BC$
- c) What is shrinkage fault and appearance fault of PLA? 14+12+4]

3.

Table-1

PS	NS, Z	
	x = 0	x = 1
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D, 1
G	D, 1	C, 1
H	B, 1	A, 1

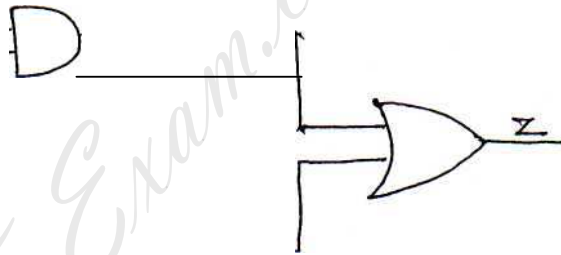
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(2) -

- a) Find the equivalence partition for the machine shown in Table-1.
 - b) Find a minimum length sequence that distinguishes state A from state B.
 - c) Find minimal form of above machine.
 - d) Explain redundancy with circuit diagram. [6+6+4+4]
4. a) What are the differences between Ad-hoc approach and structured approach of Design for testability?
- b) What are the advantages and disadvantages of LSSD method?
- c) What are the differences between scan path approach & LSSD approach? Explain with circuit diagram. [4+7+9]

5.

E» -



C

- a) Find the set of all tests that detect fault a s-a-0.
 - b) Find the set of all tests that detect multiple faults (c s-a-1, a s-a-0).
 - c) Find a counter example to the following statement:
"In a combinational circuit two fault f and g are functionally equivalent iff they are always detected by the same test". [4+6+10]
6. a) What are the advantages of Random Access scan approach in comparison to LSSD approach of DFT?
- b) Explain different modes, of BILBO register with block diagram of 8 bit BILBO register.
- c) Explain growth fault and disappearance fault of PLA. [5+10+5]
7. a) Explain stuck-open fault of CMOS circuit with diagram.
- b) What are the different stages of VHDL architecture?
- c) Explain Signature Analysis method of DFT with Block diagram. [5+7+8]