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***06* B.E. (CST) Part-II 4th Semester Examination, 2006**

System Specification and Electronic Design Automation

(CST-403)

Time : 2 hours **Full Marks : 50**

Answer FOUR** questions, **taking** TWO **from each half.** One mark is **reserved for** neatness in each **half.

FIRST HALF

1. a) i) Write the decimal number 12 3 as a sized 8 bit number in binary.
   ii) Write an unsized hex number 12 3 4 .
   iii) 4'd-2, is it specify a legal negative number?
   iv) -2 3 4 , is it illegal?

   b) Declare the following variables in verilog.
   i) An 8 bit vector net called a-in .
   ii) An integer called count.
   iii) A time variable called snap-shot.

   c) Write a verilog code of 4 :1 MUX using *2* :1 MUX. (4+3+5)

2. a) How task differ from function in verilog code?

   b) Discuss with example the application of non blocking assignment statement. (8+4)

3. a) Discuss briefly about procedural and blocking assignment statement.

   b) Discuss briefly about various methods of timing control. (6+6)

SECOND HALF

4. a) Discuss with example the difference between exit and next statement.

   b) Write down two different architecture of HALF-ADDER entity, one architecture contains sequential signal assignment statement and the other architecture contains concurrent signal assignment statement. (5+7)

5. a) Write entity-architecture for the sequential behaviour **of** R-S flip flop.

   b) Justify with example the utility of configuration statement in VHDL. (6+6)

6. a) Write a VHDL code of 1 bit full adder using mixed style of modeling.

   b) Discuss briefly about various operator in VHDL. (8+4)

Board exam question paper, sample paper, model paper, to read and download