B.E. (CST) Part-II 3rd Semester Examination, 2007

Digital Logic

(CS-301)

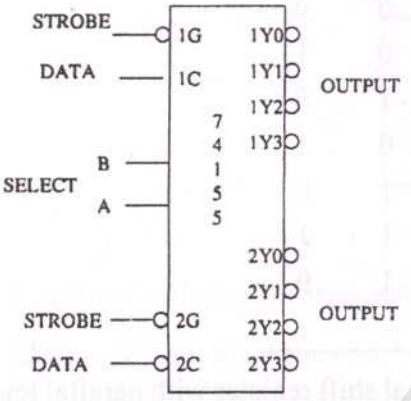
Time : 3 hours **Full Marks : 70**

Answer any FIVE questions, taking at least TWO from each group.

GROUP-A

1. a) Draw the truth table for a Half-adder. Implement the half adder using logic gates.

   b) Draw the truth table of Full-adder and implement a 4-bit adder with half adders. Extra logic gates, if required, may be used. [7+7]



a) 74155 Pindiagram

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	H	H	H	H	H

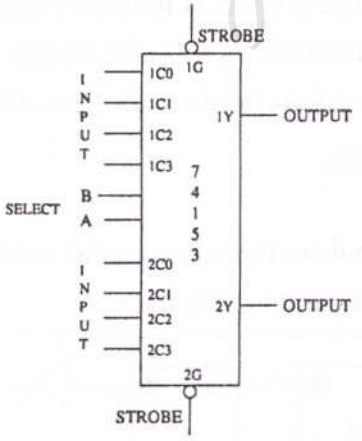
b) Function Table for 74155

Fig.-1 [Dual 1 of 4 decoder chip 74155]

2. a) Implement full adder logic with dual 2-4 decoder (74155).

   b) Implement full adder logic with dual 4 to 1 line multiplexer (74153).

   For both the cases (i.e., (a) and (b)) list the number of IC-chips and extra gates necessary to implement 4-bit adders. [7+7]



a) Pindiagram

SELECT		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

b) Function Table

Fig.-2 [Dual 4 to 1 multiplexer chip 74153]

3. a) Design a combinational circuit using a ROM (8 x 4) that accepts a 3-bit binary number and produces the square of the corresponding input value. Note that the ROM has eight locations (i.e., 3-bit address) and 4-bit outputs and the square of a 3-bit number is to be expressed in 6 bits.

   b) Derive the program table for a combinational circuit to compute the square of a 3-bit number by using PLA. Minimize the number of product terms.

[7+7]

4. a) Design the sequential circuit, whose state table is given below, using a 2-bit register and combinational gates.

Present State		Input	Next State	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

   b) Draw the circuit for a 4-bit bidirectional shift register with parallel load facility. The shift register should have clear and clock inputs as well as two mode control (s_1 and s_0) inputs. [7+7]

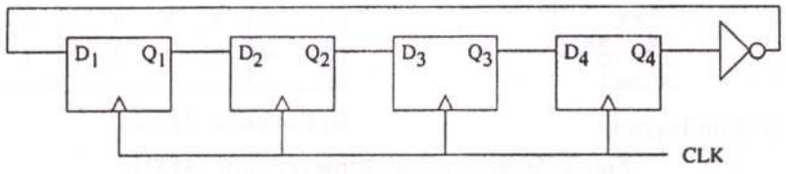
GROUP-B

5. a) Which logic level limits the fan-out of a TTL gate and why?

   b) The output of a DTL inverter is connected to other N number of similar gates. Assume that the output transistor is saturated and h_{FE} of the output transistor is 30. Find the value of N that will keep the transistor in saturation.

   c) Compare TTL and CMOS logic families. [4+6+4]

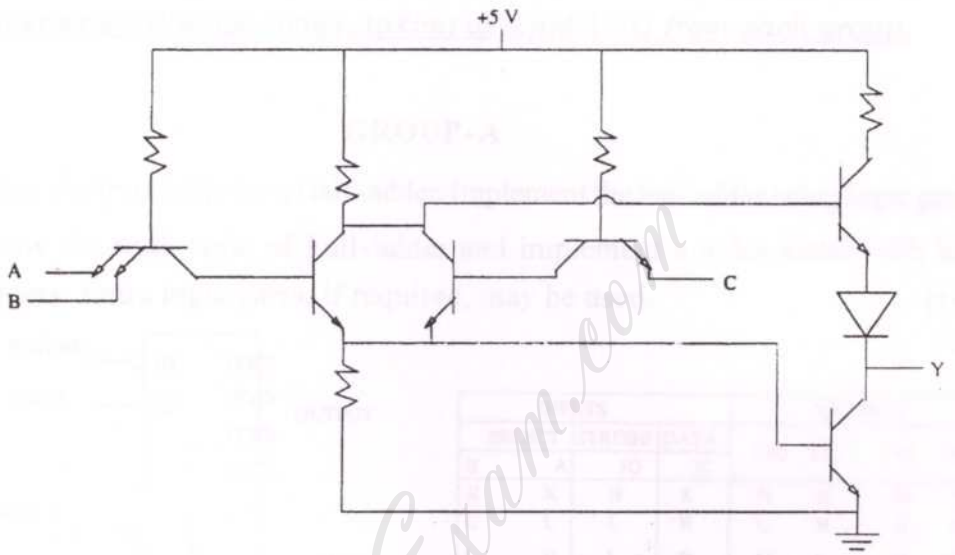
6. a) The following logic diagram is used to describe a sequential machine. Draw the state diagram depending on the assumed initial state.



b) Design a 3-bit modulo-6 gray code counter with up/down capability using J-K flip flops.

c) Design a 16:1 MUX using 4:1 MUXs. [5+5+4]

7. a) Determine the logic function for the following circuit and explain its operation.



b) Use open collector inverter gates to realize the two input exclusive OR function.

c) Define Moore machine and Mealy machine. [6+4+4]

8. a) Why can't you make S = 1 and R = 1 in an RS flip-flop? Describe the Race-around problem in level triggered J-K flip-flop.

b) A serial adder uses 2 shift registers and a flip flop. Draw the logic diagram and explain its operation. [(4+4)+6]

— — —