4th Semester Final Examination 2007
Subject :Electronic Design Automation (CS404)

Time : 2 hours FM : 35

(i) Answer two from each half
(ii) Three marks reserve for neatness

Group-A

1(a) What are the basic design methodology in verilog HDL? Discuss with example. 3
(b) A full subtractor has three 1 bit inputs P,Q,R (previous borrow). Write the full verilog description for the full subtractor module, including I/O ports. Instantiate the subtractor inside a stimulus block and test all eight possible combinations of P, Q and R. 5

2(a) What is procedural continuous assignment? Discuss about the different types of procedural continuous assignment. 5
(b) Using assign and deassign statements, design a positive edge triggered D-FF with asynchronous clear (q=0) and preset (q=1). 3

3(a) How to override the parameter values in a module? 3
(b) Build the fulladd4 module with defparam statements to change instance parameter values. 5

Group-B

4(a) What are the differences between function and procedure in VHDL? 3
(b) What is the use of package declaration and package body? 3
(c) How configuration declaration differs from configuration specification? 2

5(a) What is the basic difference between data flow style of modeling and behavioral style of modeling. What is the function of the process statement in a behavioral style of modeling? 2+2
(b) Discuss with example, the use of next, exit, wait and null statement in VHDL code. 4

6 Write a VHDL code for 3 bit bidirectional shift register. 8