B. E. Part II (CST) 4th Semester Examination, 2007

Subject: Computer Organization | Paper: CST-402

Time: 3 hours | Full marks: 70

Answer any 4

1. a) Describe the opcode extension scheme for optimizing the opcode length of an m/c instruction set. 10

   b) Show the design of a 4k X 16 RAM chip with four 2k X 8 memory unit. 7.5

2. a) State Booth's algorithm for multiplication of two 2's complement numbers. Let multiplicand Y=1010 and multiplier X=1011 and both the X & Y are represented in 2's complement. Find product P = YX following Booth's algorithm. 14

   b) Explain in brief the register indirect addressing of operands. 3.5

3. a) Identify the major differences between asynchronous and interrupt driven data transfer schemes. Give examples. 10

   b) What is `cycle stealing' DMA data transfer scheme. Comment on its effectiveness in data transfer from an Input device to the Main memory. 7.5

4. Illustrate the `diagonal format' of encoding micro-instructions for a microprogramed control unit with an example. Find out the cost optimal micro-instruction format for a system with the following set of micro-instructions and controls. Ensure minimum length of the micro-instruction format as well as the maximum parallelism among the microoperations.

Micro-instructions	Control signals
I_1	b, e, f
I_2	a, b, c, d
I_3	a, b, e, h
I_4	b, e, g

17.5

5. a) Assume that time required for the four functional units (of an instruction pipeline), which operates in each of the 4 cycles, are as follows:

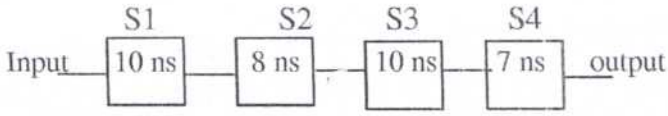

Figure 1

i) Find the reservation table for this pipeline architecture.
ii) How much speedup in the instruction execution rate will be gained in the pipeline of Figure 1 over the non-pipelined architecture. Ignore any latency impact.
iii) Suggest how speed mismatch among the pipeline stages of Figure 1 can be managed. 10

b) Consider the following reservation table for a 4-stage (S_1, S_2, S_3, and S_4) non-linear pipeline:

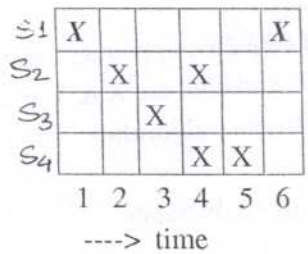

Figure 2

i) Find out the forbidden latencies of this pipeline.
ii) Give the block diagram for the non-linear pipeline architecture. 7.5

6. a) Define m-way set associative mapping. A computer system has a 128 byte cache. It uses 2-way set associative mapping with 8 bytes in each block. The physical address size is 16-bit and the word size is 1 byte.

i) Draw a diagram showing the organization of the cache indicating how physical addresses are related to cache addresses.
ii) To what block frames of the cache can the address 20FFh be assigned?
iii) Point out the advantage of 2-way set associative mapping over 1-way set associative mapping. 10

b) What is CAM? Find out the expression of match logic of a CAM. 7.5

7. Give the detailed design of the following:
a) Memory interfacing with complete decoding 10
b) Addition of 6 n-bit numbers with Carry Save Adders 7.5