B.E. (CST) Part-II 3rd Semester Examination, 2007

Electronic Devices & Circuits

(ET-305)

Time : 3 hours **Full Marks : 70**

Use separate answerscript for each half.
Answer SIX questions, taking THREE from each half.
Two marks are reserved for neatness in each half.

FIRST HALF

1. a) What do you mean by intrinsic semiconductor? What is the position of the Fermi level in a intrinsic semiconductor? How does its position change when (i) donors and (ii) acceptors are added to the semiconductor?

   b) Define the mobility of charge carriers in a semiconductor. Obtain expressions for electrical conductivity of (i) an intrinsic, (ii) p-type semiconductor.

   c) Give the theory of Hall effect? A rectangular n-type semiconductor specimen of width 1 mm carrying a current of 10 mA is placed in a transverse magnetic field of 0.2 T. If the Hall voltage is 20 mV, calculate the electron concentration in the sample. [11]

2. a) Draw the energy-band diagram of an open-circuited p-n junction. Explain the following terms with reference to a p-n junction : uncovered charges, barrier field, depletion region and potential barrier.

   b) What is the origin of the reverse saturation current in a p-n junction? Does the reverse saturation current change with the applied reverse bias and the diode temperature? Explain.

   c) Discuss the origin of breakdown of a p-n junction? What is the difference between avalanche breakdown and Zener breakdown of a p-n junction?

   d) The reverse saturation current of a Si p-n junction is 5 mA at 27°C. What are the static and the dynamic resistances of the junction for an applied forward bias of 0.6 V? [11]

3. a) Why are junction transistors called bipolar devices? Why is the emitter region of a transistor more heavily doped than the base region? Why is the width of the base region very thin?

b) Explain the current amplification factor α and β for common emitter configuration. If $\beta = 16.5$, $I_E = 1.8\,mA$ and $I_{CO} = 12\,\mu A$, calculate I_C and I_B when the transistor is used in CE configuration.

c) What is a bias curve? How is the Q-point in a self-bias circuit determined with and without the help of a bias curve? Find out the Q point of a self bias circuit with following specifications :
$V_{CC} = 22.5\,V$, $R_L = 5.6\,k\Omega$, $R_e = 1\,k\Omega$, $R_1 = 90\,k\Omega$, $R_2 = 10\,k\Omega$, $V_{BF} = 0.7\,V$ and $\beta = 55$. Assume $I_B \gg I_{CO}$. [11]

4. a) Draw the circuit diagram of a two stage RC-coupled CE transistor amplifier. Show how the magnitude and the phase angle of its voltage gain vary with frequency. Define the half-power frequencies.

b) The mid frequency gain of an RC-coupled amplifier is 100. The lower half-power frequency is 50 Hz and the upper half power frequency is 200 kHz. At what frequencies is the gain 80?

c) What are the special features of a power transistor? Explain with a circuit diagram the operation of a push-pull power amplifier. Obtain an expression for the maximum efficiency of the circuit. [11]

5. a) What is the Barkhausen criterion? State the basic conditions for oscillation in a feedback amplifier.

b) Describe with a circuit diagram to Wien bridge oscillator. If it has a resonant frequency of 1 kHz and a capacitance of 100 pF. Find the resistance. If the amplifier gain is 10, obtain the ratio of the resistance in the other arms.

c) Describe the principle of operation of a crystal oscillator. Mention its advantages. Draw the equivalent electrical circuit of a piezoelectric crystal. If $L = 3\,H$, $C = 0.05\,pF$, Mounting capacitance $(C_M) = 6\,pF$ and $R = 1000\,\Omega$. Determine the series and parallel resonant frequencies. Also find the Q factor of the crystal. [11]

SECOND HALF

6. a) With a neat sketch, describe the construction of an n-channel junction field effect transistor (JFET). Explain its principle of operation.

b) Explain the nature of the typical common-source drain characteristics of a JFET. What is its transfer characteristic? How do the saturation voltage and saturation current vary when the reverse gate-bias increases?

c) Define pinch-off voltage. Sketch and explain the characteristics depletion region before and after pinch-off. [11]

7. a) Sketch the structure of an n-channel depletion type MOSFET. Explain how the depletion region is produced in the channel.

b) How can one use an n-channel MOSFET in either the enhancement or the depletion mode? Explain the corresponding voltage-ampere characteristics.

c) Draw the drain-to-gate bias circuit diagram of an enhancement MOSFET. Show how the gate-source junction is forward-biased. [11]

8. a) What is negative feedback? Why is it so much used in operational amplifier circuit.

b) Define desensitivity factor, and loop gain of a feedback amplifier. State the effects of negative feedback in an amplifier.

c) The open loop gain of an amplifier changes by 5%. If 10 dB negative feedback is applied, calculate the percentage change of the closed loop gain. [11]

9. a) Draw the noninverting voltage feedback circuit and derive the expression for closed loop voltage gain.

b) How do input impedance and output offset voltage of an op-amp change will non inverting voltage feedback?

c) How we can reduce output offset voltage by inserting a bypass capacitor in the feedback loop.

d) How we can change the voltage gain by using JFET-switch. Explain with necessary circuit diagram. [11]

10. Write short notes on (any two) of the following : [5½×2]

i) Active peak detector circuit
ii) Schmitt trigger circuit
iii) Op-Amp differentiator
iv) Current booster circuit of Op-Amp.

— — —