Ex/BESUS/EE-403/06

B.E. (EE) Part-II 4th Semester Examination, 2006

Solid State Devices and Circuits-I

(EE-403)

Time : 3 **hours** **Full Marks** : **100**

Use separate answerscript for each half.
Answer SIX questions, taking THREE from each half.
Two marks are reserved for neatness in each half.

FIRST HALF

1. a) Find the transfer characteristic of the diode circuit shown in Fig.-1. Consider diode Dl is an ideal diode.

   b) If a resistive element of resistance lOkQ is connected across the terminal 1-2, what will be the change in the transfer characteristic.

   c) What will be the effect of diode capacitance on the clipping circuit shown in Fig.-1.

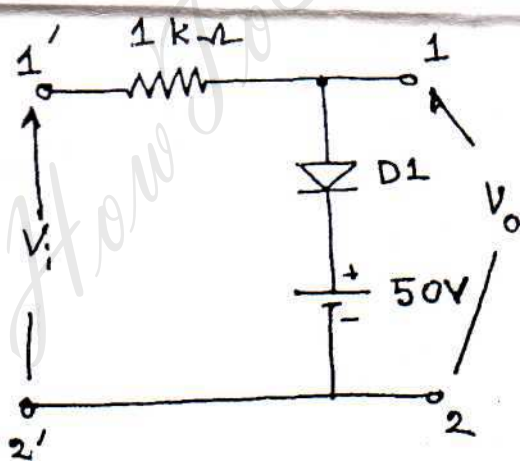


Fig.-l

2. a) Design a full wave bridge rectifier circuit which will convert 220 V, 50 Hz AC input to a DC voltage supplying 50 ohm resistive load.

   b) How can you ripple in the output of a rectifier?

   c) What is the role of Zener diode in regulating the dc voltage obtained from a rectifier output? [6+4+6]

3. a) Explain the output characteristic of JFET.

b) A JFET amplifier is shown in Fig.-3. I_{DSS} for the JFET is 1.65 mA and the gate-source pinch-off voltage V_P = -2.0 V. Find the voltage amplification. Assume r<j»R_L. (8+8]

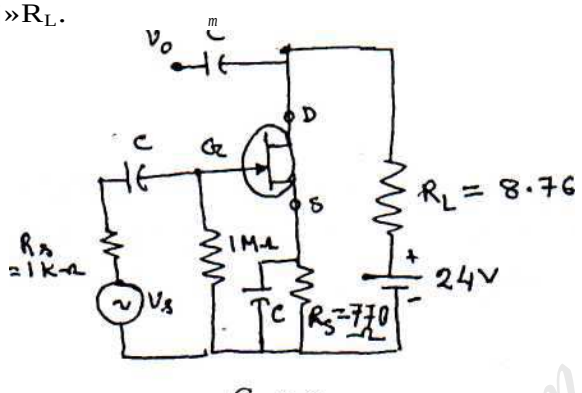


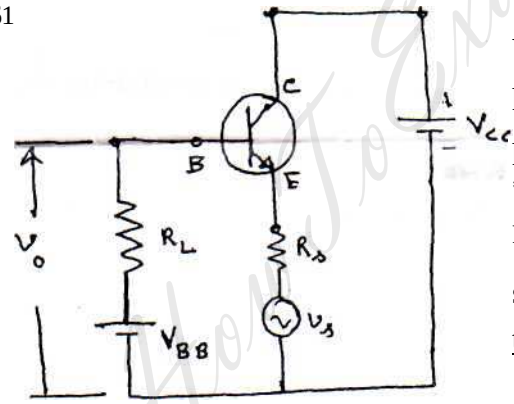
Fig.-3

4. a) What do you mean by biasing of a FET?

b) Explain the operation of an universal biasing circuit for FET.

c) A circuit is shown in Fig.-4. Is it an amplifier circuit? Justify your answer.

[4+6+61



Vs -» input signal

h_{fe}>l

h_r

*re

Fig.-4

Write short notes [8+8]

on any two :

a) Enhancement type MO S FET

b) Depletion type MOSFET

c) Peak detector circuit using diodes

d) Voltage multiplier circuit using diodes and capacitors.

SECOND HALF

6. Express CB h-parameters of a BJT in terms of CC h parameters. Hence evaluate the CB h parameters, if for a typical BJT, it is given that,

hj_c = 1.1 kQ ; h_{rc} - 1 ; hf_c = - 51 ; h_{oc} = 25 u^

Draw both the h-parameter equivalent circuits. [3x4+4]

7. a) For the transistor shown the h-parameters with the respect to the E terminal (i.e., CE h-parameters) are as below

h_{ie} = 1.1 kQ ; h_{re} = 0.25 x 1(T^3 ; h_{fe} = 50; h_{oe} = 2

Find the modified h parameters h'j_e, h'$_{re}$, h'f_e and h'$_{oe}$ (with respect to the E' terminal) after deriving expressions for the same. Take R_e = 1.0 kQ.

b) From the Taylor series representations of input and output characteristics derive the CE-h parameter model of a transistor.

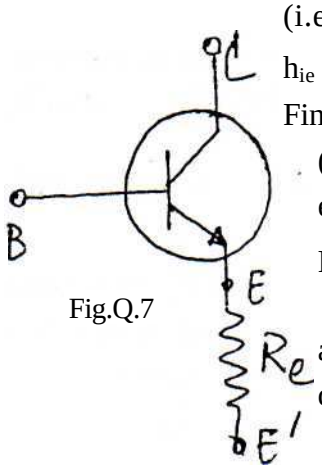


Fig.Q.7

8. a) Identify what type of circular has been used in the biasing section of the transistor circuit shown in Fig.-9. Derive an expression relating I_c and V_{BE} and discuss the effects of variation of temperature on collector current I_c. How is it better than other biasing schemes?

b) Derive expressions for the stability factor SI and the stabilisation factors S2 and S3. Discuss about the ranges in which their values may lie.

c) What are output and input-non-linear distortion with respect to a transistor working as an amplifier? Explain with relevant waveforms. How can distortion be reduced? [5+6+5]

9. a)

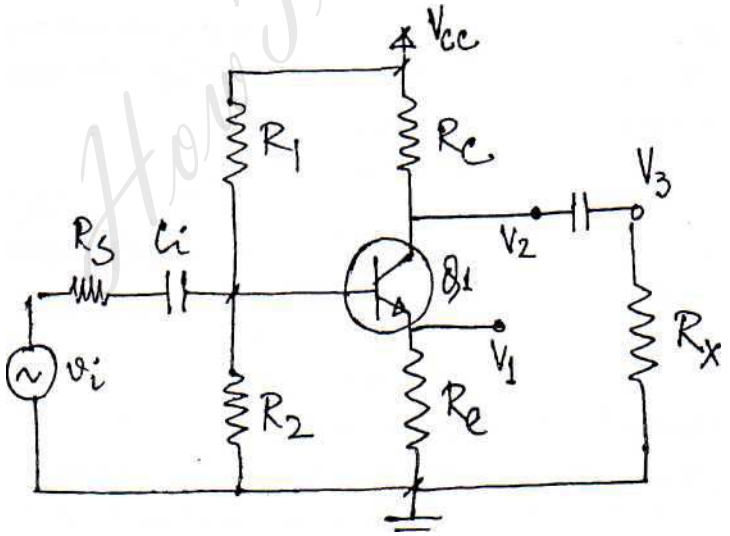


Fig.9

For the transistor Ql based circuit in Fig.-9 the nominal point of operation is to be located at V_{CE} - 14V and I_c - 1.6 mA with SI < 4. Assuming that

P - 80, V_{BE} = 0.7 V, V_{cc} = 18 V and R_c = 3.9 kQ design suitable values of R_e, Rj and R_2. Evaluate S_2 also.

b) If the value of R_e as found in part (a) above is set to zero determine (i) the zone of operation of the transistor (ii) the values of I_c, Vj and V_2. [9+7]

10. a) Identify the component shown by a dashed box in figure Fig.-lO(a). If Vj is a 5.0V square pulse of 1 kHz frequency

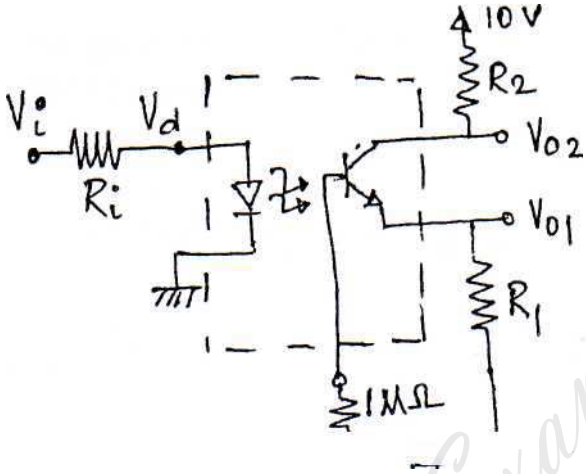


Fig.-lO(a)

i) Find the value of Rj so that a maximum of 20 mA can pass.

ii) Assuming that the transistor stage works like a switch plot Vj, V_{01} and V_{02} one below the other for R_2 = 0,R,*0.

*i ------J2.—**

iii) Repeat part (ii) for R, = 0 [anc]* R2*0.

iv) Plot Vj and V<j against time, assuming reasonable value of diode voltage drop in the on-state.

b) For the schematic connection diagram shown in figure Fig.-lO(b) involving an 1EM Hall Current Sensor determine

i) the recommended pin connections to measure 8-12-25A, with proper justification

ii) the value of the measuring resistance if corresponding to 25 A (r.m.s.) primary current (a.c.) the output voltage has to be around 4.5 V

iii) Principle involved in sensing current.

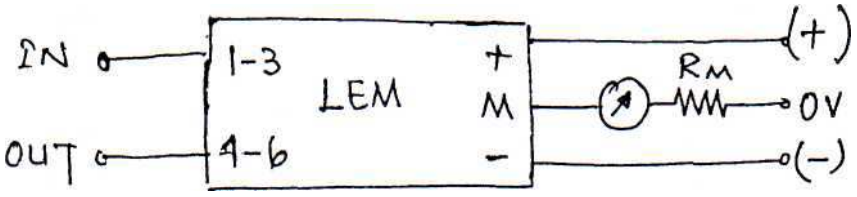


Fig.-lO(b)

The datasheet of the current sensor is as below :

I_{PN} (primary nominal RMS current) = 25 At, I_P (primary current measuring range) = 0-55 At, R_M (measuring resistance at 70°C) = 0 to 155 Q (with ± 12 V) and 67 to 236 Q (with ± 15 V). Secondary nominal rms current =

25 mA, K_N (conversion ratio) = 1/2/3:1000, supply voltage = ± 12 to ± 15 V.

[9+7]