Ex/BESUS/EE-404/07

B.E. (EE) Part-II 4th Semester Examination, 2007

Solid State Devices and Circuits-I

(EE-404)

Time : 3 hours **Full Marks : 70**

Use separate answerscript for each half.
Answer SIX questions, taking THREE from each half.
Two marks are reserved for neatness in each half.

FIRST HALF

1.

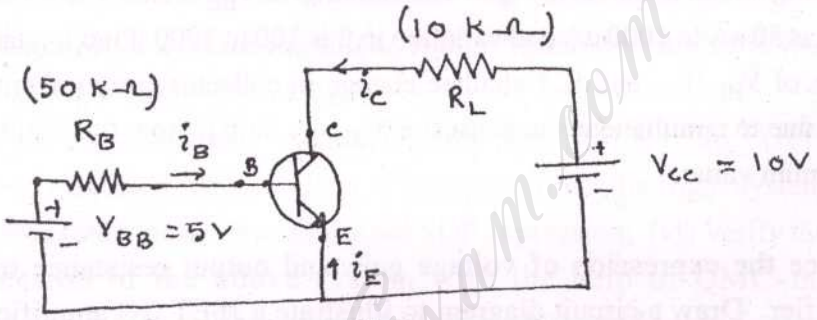

Fig.1

A BJT transistor circuit is shown in Fig.1. Represent the circuit by replacing the transistor with its Ebers-Moll model. Given that $\alpha_F = 0.96$, $\alpha_I = 0.1$, $|I_{CO}| = 10$ nA, $|I_{EO}| = 1.1$ nA. Volt-equivalent of temperature (V_T) = 0.026 V, base-emitter voltage drop $v_{BE} = 0.75$ V. Find i_B, i_C and i_E. Find also Large signal α (alpha) and β (Beta) of the transistor. What is the collector voltage with respect to base?

[3+4+2+2]

2.

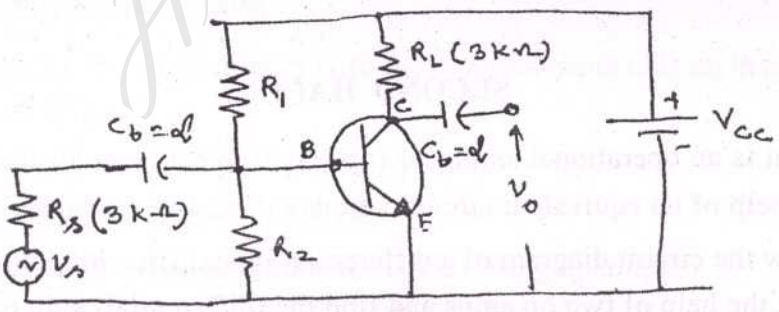

Fig.2

A CE BJT amplifier is shown in Fig.2. The h-parameter values are $h_{ie} = 1{,}100\ \Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$ and $1/h_{oe} = 40\ k\Omega$. Find the voltage gain and the current gain of the amplifier. Neglect the effect of biasing circuit. If a capacitor of infinite capacitance is connected between collector and emitter, find the voltage gain and current gain of the circuit.

[4+3+2+2]

3.

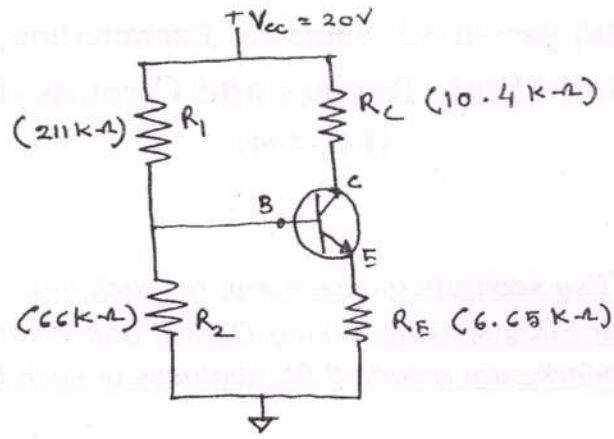

Fig.3

A biasing circuit is shown in Fig.3. The variation of V_{BE} is 0.65 V to ± 100 mV, variation in I_{CO} is 50 nA to 1000 nA and variation in β is 100 to 1000. Find I_{CQ} taking minimum values of V_{BE}, I_{CO} and β. Calculate change in collector current from the quiescent value due to simultaneous increases of V_{BE}, I_{CO} and β from their minimum value to maximum value. [4+7]

4. Deduce the expression of voltage gain and output resistance of a JFET CD amplifier. Draw a circuit diagram to illustrate a JFET CG amplifier. In which of the two amplifiers, the input resistance is more? [5+3+3]

5. Write short notes on any two : [5½+5½]
   i) Gate-source pinch-off voltage
   ii) Current saturation in JFET
   iii) Inverter logic circuit using CMOS
   iv) Universal Biasing circuit for FET.

SECOND HALF

6. a) What is an operational amplifier (op.amp)? What is an ideal op.amp? With the help of its equivalent circuit compare these two op.amps.
   b) Draw the circuit diagram of a differential input differential output amplifier with the help of two op.amps and find the (differential) gain of the circuit.
   c) Draw the circuit diagram of a non-inverting gain amplifier with gain more than unity and find the expression of gain. [4+4+3]

7. a) What is an integrator? With the help of circuit diagrams express input output relation of (i) passive– and (ii) active– integrators using RC components. Compare the two.

b) What is a regenerative analog comparator circuit? Draw its transfer characteristics and label the important nodes in the diagram.

c) Using regenerative comparator and RC components, draw the circuit diagram of a square wave oscillator using op.amp and develop the expression of time period of output. [3+4+4]

8. a) A logic system is described with the help of a min-term expression as follows :

$$Y(A, B, C, D) = \sum m\,(0, 5, 11, 14) + d(1, 4, 7, 10, 13, 15)$$

Find out the minimal logic expression and realise the system with the help of AND-OR configuration.

b) The function of a Three-input (A, B, C) digital system (Y) is described as $Y(A, B, C) = \Pi M(1, 0)$.

Draw its (i) truth table; (ii) Venn diagram; (iii) K-map; (iv) min-term (SOP) expression (extended); (v) Now minimise the logic system with the help of K-map to have its minimised SOP expression; (vi) Verify the minimal expression of the above system with the help of QMC-method of minimisation; (vii) Now using NAND-NAND configuration represent the minimal logic circuit of the system; (viii) Also draw the realised logic system using single 4 line – 1 line MUX. [3+8]

9. a) What is a multiplexer? Draw the internal logic circuit of a single 4 line – 1 line multiplexer (without STROBE).

b) Represent a 2-in XOR gate using four (4) 2-in NAND gates and show its performance analytically.

c) Realise a 2-bit word squarer with BCD output using only an inverter and two 2-in AND gates. [4+4+3]

10. Write technical short notes on <u>any two</u> : [5½+5½]

a) Any two active analog subtractor circuit using op.amps.

b) Three input adder circuit and its I/O relations.

c) An astable multivibrator using Op.amp.

d) TTL NAND gate with Totempole output and open collector output.

e) N-Ch MOS inverter and CMOS inverter.

f) Full Adder circuits and its use in a 4-bit parallel adder.

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